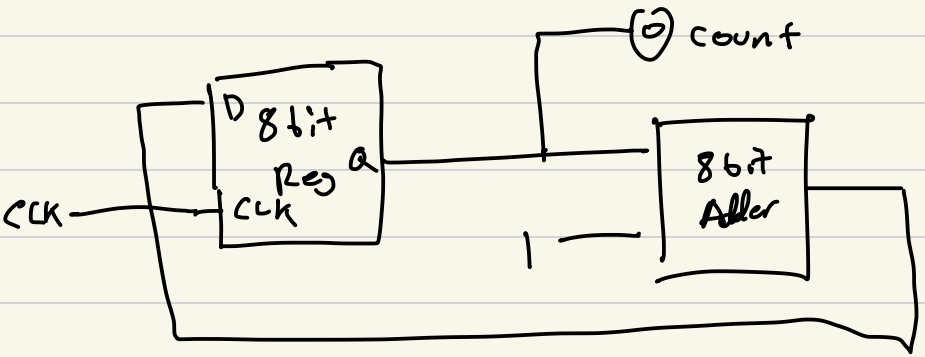
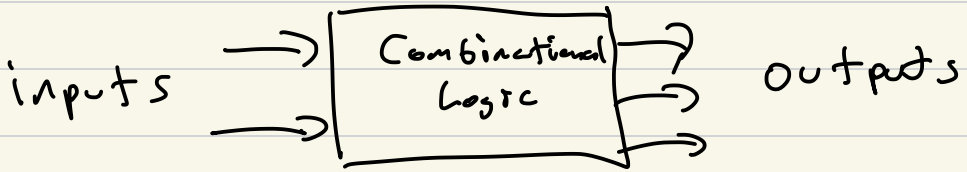
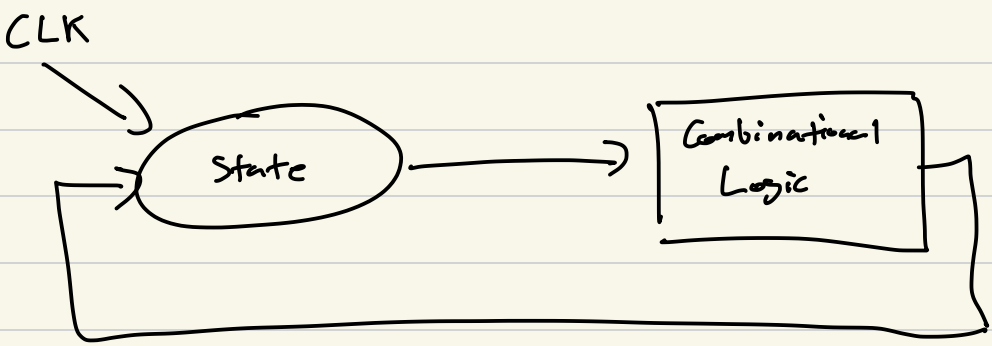
CS 315-02 Lab Sequential Logic Registers

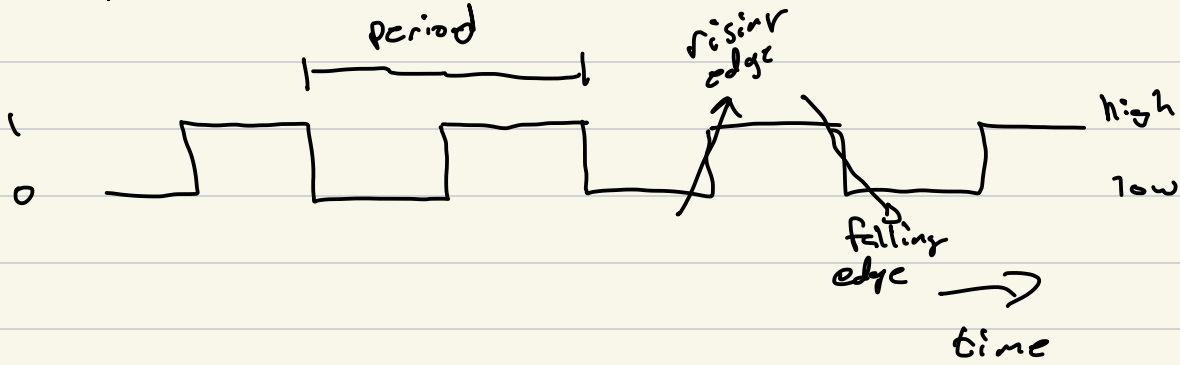




function



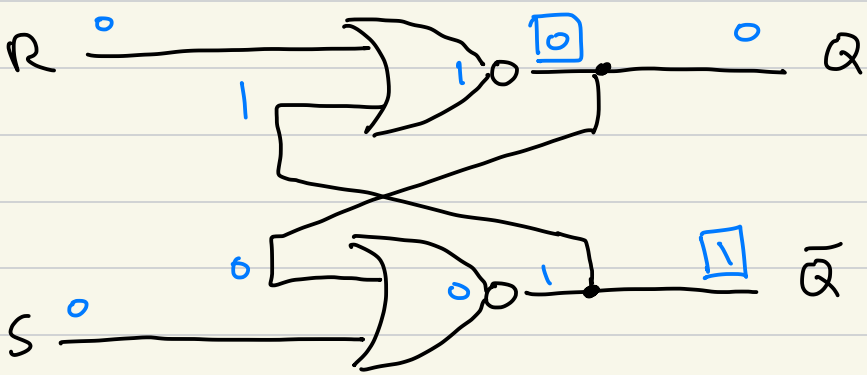
Clock cycle

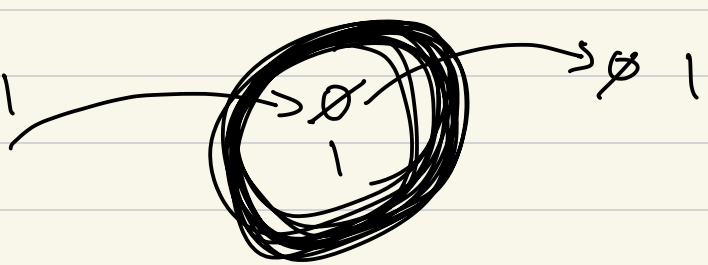


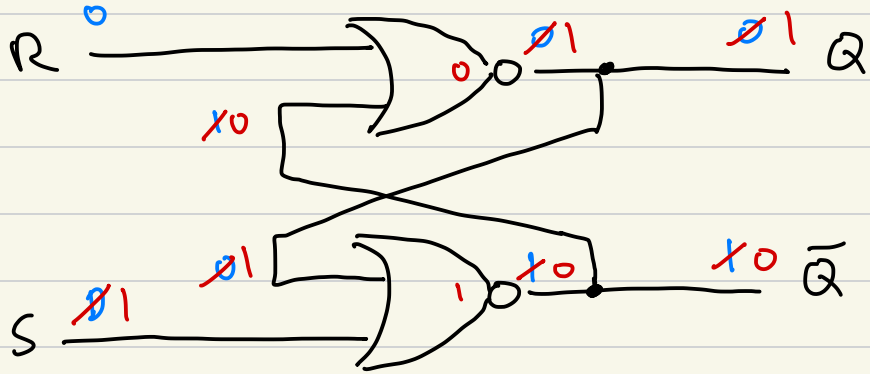
How to store a 1 bit value

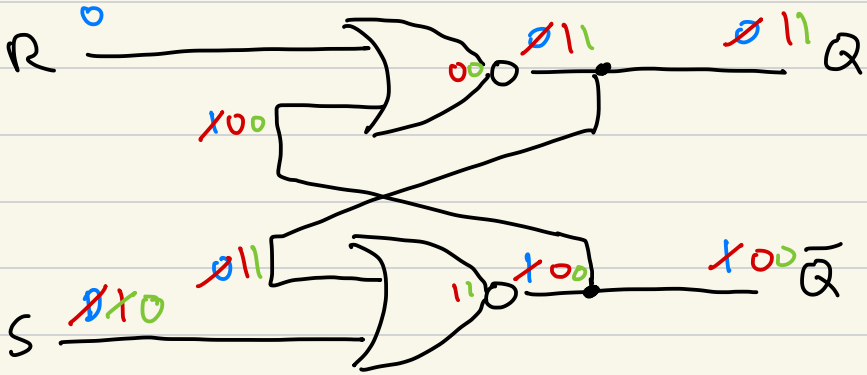
S R Latch Set / Reset

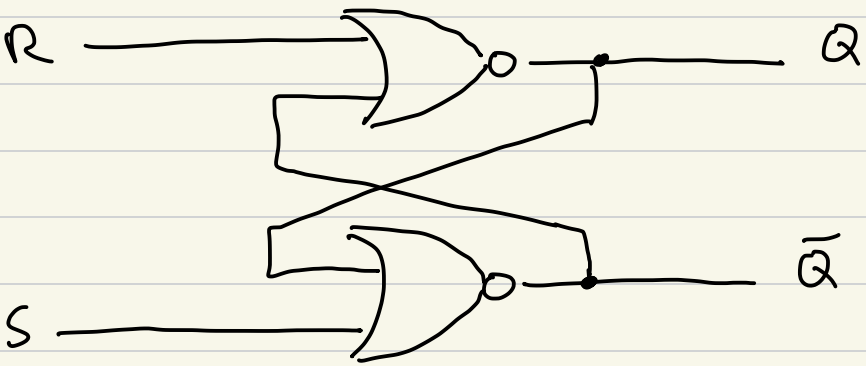
NOR Gate






R
S
Q
$\bar{Q}$


R
S
Q
$\bar{Q}$


R
S
Q
$\bar{Q}$

time ↓

R	S	Q	$\bar{Q}$	
0	0	0	1	
0	1	1	0	
0	0	1	0	
1	0	0	1	
0	0	0	1	
1	1	X	X	undefined

SR Latch

D Latch

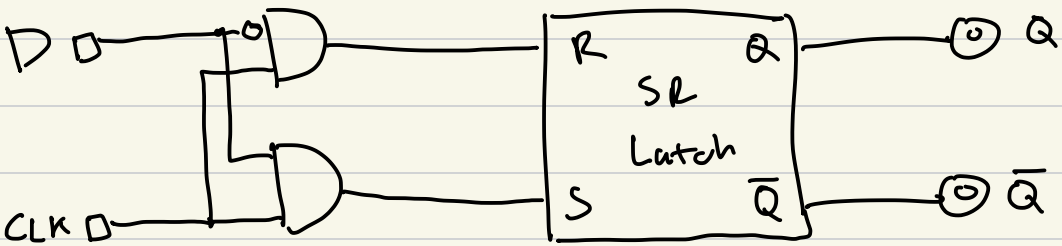
D Flip-flop

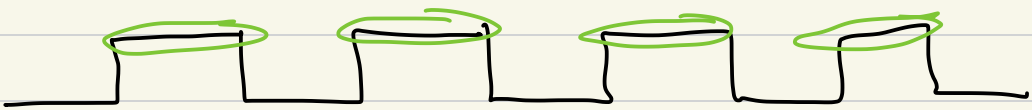
1-bit Register

N-bit Register

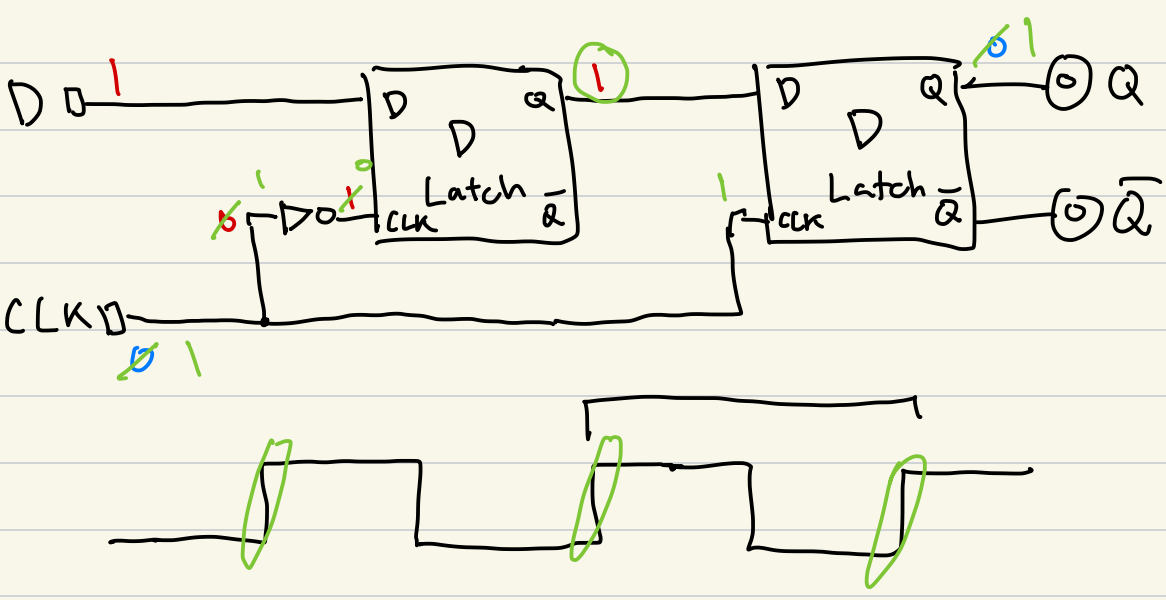
Counter

D Latch



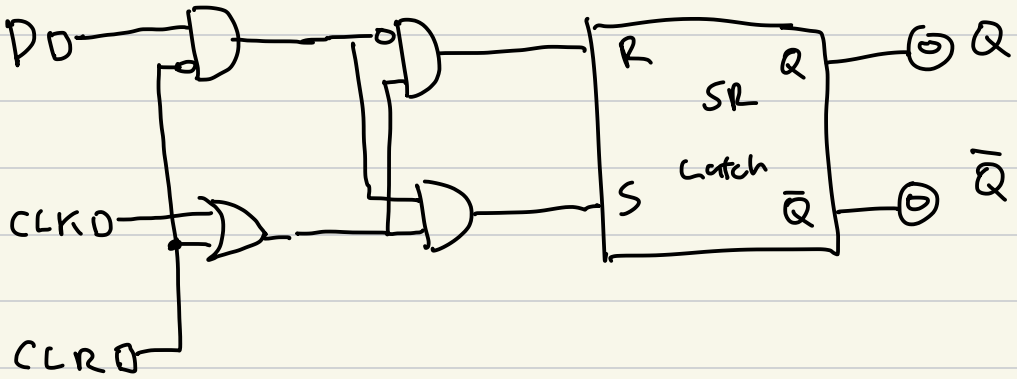


D Flip-flop

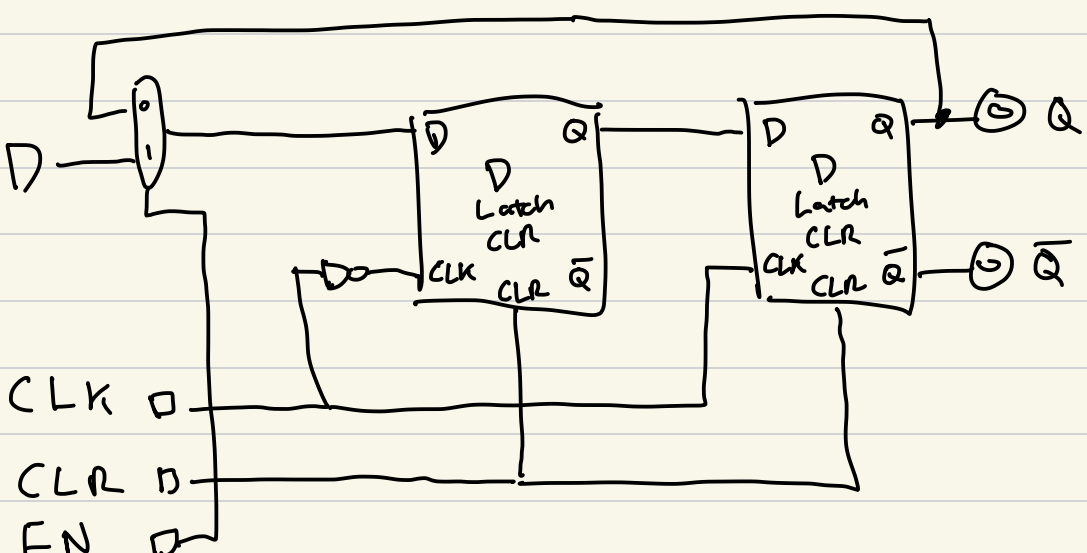


1 bit register

D Latch with CLR



1 bit register



4 bit Resister